CLAIMS

What is claimed is:

1. A circuit substrate, comprising:

a board having a plurality of conductive traces layers and insulating layers, and a via formed in the board;

a plurality of metal layers formed on an inner wall of the via, wherein each of the metal layers electrically connects to said corresponding conductive traces layer respectively; and

an insulator formed in the via to electrically isolate from each of the metal layers.

2. The circuit substrate of claim 1, further comprising a plurality of via lands disposed on the board and at the periphery of the via.

3. The circuit substrate of claim 2, wherein each of the via lands is disposed correspondingly to each of the metal layers.

4. The circuit substrate of claim 1, wherein the insulator is positioned between the metal layers.

5. The circuit substrate of claim 1, wherein the via is a through hole.

6. The circuit substrate of claim 1, wherein the via is a buried via.

7. The circuit substrate of claim 1, wherein the via is a blind via.

8. The circuit substrate of claim 1, wherein the material of the metal layers is copper.

9. The circuit substrate of claim 1, wherein the material of the insulator is epoxy.

10. The circuit substrate of claim 1, wherein the material of the insulator is ink.

11. The circuit substrate of claim 1, wherein the board comprises a plurality of insulating layers and conductive traces layers, and the insulating layers are interlaced with the conductive traces layers.

12. The circuit substrate of claim 2, wherein the via land is made of copper.

13. A fabrication method of a circuit substrate, comprising:

providing a board;

forming a via in the board;

forming a metal layer on an inner wall of the via;

cutting the via to form a cutting street to separate the metal layer into a plurality of separated metal layers; and

filling an insulator in the via and the cutting street.

14. The fabrication method of a circuit substrate of claim 13, further comprising:

forming a via land on the board and at the periphery of the via.

15. The fabrication method of a circuit substrate of claim 14, wherein cutting the via further separates the via land into a plurality of separated via lands.

16. The fabrication method of a circuit substrate of claim 13, wherein the via is a through hole.

17. The fabrication method of a circuit substrate of claim 13, wherein the via is a buried via.

18. The fabrication method of a circuit substrate of claim 13, wherein the via is a blind via.

19. The fabrication method of a circuit substrate of claim 13, wherein the material of the metal layer is copper.

20. The fabrication method of a circuit substrate of claim 13, wherein the material of the insulator layer is epoxy.

21. The fabrication method of a circuit substrate of claim 13, wherein the material of the insulator layer is ink.

22. The fabrication method of a circuit substrate of claim 13, wherein the board comprises a plurality of insulating layers and conductive traces layers, and the insulating layers are interlaced with the conductive traces layers.

23. The fabrication method of a circuit substrate of claim 13, wherein forming the metal layer on the inner wall of the via comprises:

forming an activated film on the inner wall of the via by electro-less plating; and

forming a metal film on the activated film by plating.

24. The fabrication method of a circuit substrate of claim 23, wherein the activated film comprises a conductive polymer film.

25. The fabrication method of a circuit substrate of claim 13, wherein cutting the via comprises mechanical drilling.

26. The fabrication method of a circuit substrate of claim 13, wherein cutting the via comprises laser ablation.

27. The fabrication method of a circuit substrate of claim 13, wherein cutting the via comprises photochemical reaction.

28. The fabrication method of a circuit substrate of claim 13, wherein cutting the via comprises plasma etching.